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(54) **Isolated vertical PNP transistor and a process for fabricating the same**

Isolierter vertikaler PNP-Transistor und Verfahren zu seiner Herstellung

Transistor PNP vertical isolé et sa méthode de fabrication

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Description

FIELD OF THE INVENTION

[0001] This invention relates to improvements in semiconductor integrated circuit fabrication processes, or the like, and more particularly to improvements in processes for making vertical PNP transistors, which may be performed in conjunction with other semiconductor fabrication processes, especially BiCMOS and related processes.

BACKGROUND OF THE INVENTION

[0002] Many mixed-signal BiCMOS processes today are based on N well CMOS, BiCMOS, LinCMOSÔ, or LinBiCMOSÔ starting processes. In linear mixed-signal device fabrication processes, it is often necessary to use isolated complementary, or CMOS, devices in the designs to be accomplished. In many linear applications, however, bipolar devices are preferable to CMOS devices, due to the higher transconductance, improved noise performance, and 'voltage-handling capabilities of such bipolar devices. It is evident, of course, that the provision of vertical PNP transistors in addition to traditional vertical NPN transistors, which are easier to construct, would be extremely useful. However, N well CMOS processes do not easily lend themselves to building isolated vertical PNP devices. In fact, isolated vertical PNP transistors have not been commonly constructed in conventional bipolar processes that use N type epitaxially grown silicon.

[0003] As a result, when a PNP transistor is needed in N well processes, designers frequently construct isolated lateral PNP transistors. Isolated lateral PNP transistors, however, have many disadvantages. Commonly, for example, isolated lateral PNP transistors have a low frequency threshold (F_t) due to the long base widths dictated by the lithography used in the device manufacturing process. Isolated lateral PNP transistors also commonly have an early onset of high-current injection due to lightly doped base regions when the N well diffusion serves as the base. Finally, isolated lateral PNP transistors generally require a relatively high ratio of device size to substrate area. Historically, the lack of a suitable PNP transistor has hampered analog designs, resulting in elaborate schemes to shield the slow, isolated, lateral PNP transistors from the signal path. This was sometimes possible, but in many instances it was not.

[0004] Despite the trend toward construction of lateral PNP transistors when they are needed, vertical, or substrate, PNP transistors generally can be constructed in N well BiCMOS processes. However, they are typically formed in a common collector form, which greatly limits their applicability. Furthermore, it is undesirable in most BiCMOS processes to have large substrate currents present, which would certainly be the case with substrate PNP transistors. Such substrate currents can lead to debiasing effects, increasing the potential for latchup. Thus, the lack of a suitable PNP transistor has resulted in an effective inability to merge high performance analog circuitry with digital logic, a critical requirement as the push toward mixed-signal system chips accelerates.

[0005] A method of making an isolated vertical PNP transistor in a complementary BiCMOS process with EEPROM memory is known from EP-A-0 529 860. The isolated vertical PNP transistor is formed on a P substrate with a P epitaxial layer. The collector of the vertical PNP transistor is isolated with an N buried layer formed in the P substrate and an N+ buried layer on the sidewalls for isolation. The collector is formed with a P+ layer buried in the N- layer. Subsequently, the P epitaxial layer is deposited and an N+ sinker is diffused down to the N+ buried layer to complete the isolation. The emitter of the vertical PNP transistor is formed during the same step as the P+ source/drain implant for the CMOS transistors. By forming the collector and its isolation regions in the substrate before depositing the epitaxial layer, the process is compatible with forming EEPROM which is done after the epitaxial layer is deposited. An earlier implantation of the N base layer in the front-end of the process allows a deeper base junction depth, for formation of a high voltage PNP transistor. Alternately, the base can be formed later in the process, for a low voltage transistor. The presence of both high and low voltage transistors makes integration of EEPROM on the same chip practical.

[0006] U.S. Patent 4,855,244 discloses a method of making a vertical PNP transistor in merged bipolar/CMOS technology. The transistor has a P+ buried layer as a collector region, which is isolated from the P substrate by an N- buried layer. The P+ buried layer diffuses downwards into the N-buried layer and upwards into a P- epitaxy layer and into a base region. The base region is formed in the same processing step as the N well region of a PMOS transistor and the collection region of a NPN transistor. By diffusing into the base region, the width between the collector and emitter is reduced. The emitter can be formed in conjunction with the source and drain regions of the PMOS transistor. The vertical PNP transistor is laterally isolated from the other transistor devices by an annular ring formed from an N+ region formed in conjunction with an N+ DUF region used in the NPN transistor, and an N+ region formed in conjunction with an N+ collector region of the NPN transistor. An N+ DUF region may also be used in conjunction with the PMOS transistor.

[0007] U.S. Patent 4,994,887 describes an integrated circuit having PMOS, NMOS and NPN transistors for applications in which both digital and analog circuits are required. The integrated circuit is designed to allow standard CMOS cells to be used in the integrated circuit without redesign. That document discloses forming a lightly doped P epitaxial layer on a higly doped P substrate prior to forming N+ DUF regions in a BiCMOS process.

[0008] Of course many semiconductor integrated circuit processes are quite complicated, involving the use of many masks and many process steps. It is therefore important to minimize as much as possible the 'number of masks and process steps necessary to fabricate a complete device, as each additional step or mask has a tendency to reduce the yield and reliability of final circuits.

SUMMARY OF THE INVENTION

[0009] In light of the above, therefore, it is an object of the invention to provide an improved process for making a vertical PNP transistor.

[0010] It is still another object of the invention to provide a process for making a vertical PNP transistor that does not require undue additional masks or process steps.

[0011] These and other objects, features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read in conjunction with the accompanying drawings and appended claims.

[0012] In accordance with the invention, a process for making a vertical PNP transistor is presented. The process includes the steps defined in claim 1.

[0013] Various steps in the construction of the vertical PNP transistor, such as the steps of diffusing an isolation impurity, diffusing a base impurity, and diffusing an emitter impurity process, may be performed simultaneously with corresponding steps of a BiCMOS process. In one embodiment, for example, the step of forming a tunnel diode for charge transfer to a floating gate of an EEPROM device may be performed at the same time as the step of diffusing a base impurity in the construction of the vertical PNP device.

[0014] In the construction of the PNP transistor, the step of implanting an emitter impurity of the second conductivity type into the exposed emitter region may be performed by implanting boron, and the step of implanting a base impurity of the second conductivity type into the exposed well region may be performed by implanting antimony.

BRIEF DESCRIPTION OF THE DRAWING

[0015] The present invention will now be further described with reference to the accompanying drawings, in which;

Figures 1a - 1h are cross sectional side views of a portion of an integrated circuit, showing the sequence of fabrication steps in the construction of an isolated vertical PNP transistor, in accordance with a preferred embodiment of the invention;

Figure 2 is a graph taken at B-B in Figure lh showing a doping concentration profile as a function of depth into a vertical PNP transistor from its surface, in accordance with a preferred embodiment of the invention;

Figure 3 is an enlarged portion of the graph of Figure 2, showing the effects of a collector resistivity adjusting implant on the base width of a resulting PNP transistor, in accordance with one aspect of a preferred embodiment of the invention;

Figures 4a and 4b are cross sectional drawings of a portion of an integrated circuit in which a few device structures that are typically found in many BiCMOS processes are illustrated in combination with a vertical PNP transistor constructed in accordance with the invention to show some of the process steps that may be simultaneously performed;

Figure 5 is a cross sectional drawing of a portion of an integrated circuit showing an isolated vertical PNP transistor, without a collector resistivity implant, in which a donor impurity has been introduced adjacent the base region to improve the voltage handling capability of the PNP transistor; and

Figures 6a and 6b cross sectional drawings of a portion of the integrated circuit of Figure 5 showing the performance of preliminary surface doping and counter doping to selectively dope the upper portion or surface region of the epitaxial collector of the PNP transistor.

[0016] In the various figures of the drawings, which are not necessarily drawn to scale, like reference numerals are used to denote like or similar parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] It should be noted that the process steps and structures herein described do not necessarily form a complete process flow for manufacturing integrated circuits. It is anticipated that the present invention may be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention.

[0018] According to a preferred embodiment of the invention, a process is presented for making a vertical transistor, and in particular, a vertical PNP transistor in a doped semiconductor substrate of a first conductivity type. The steps in the process are illustrated in sequence in Figures 1a - 1h, which are cross sectional side views of a portion of an integrated circuit. The resulting vertical PNP transistor is shown in Figure 1h.

[0019] The process for making the vertical PNP transistor may be, and is preferably performed in conjunc-

tion with a typical process for making mixed-signal BiCMOS structures. Thus, in a typical process for making mixed-signal BiCMOS structures, a silicon semiconductor substrate 10 is provided, which has been heavily doped with an acceptor impurity, such as boron, or the like, to have a P+ type conductivity, as shown in Figure la. In a typical CMOS or BiCMOS process, a first layer 12 of semiconductor material that has been lightly doped with a donor impurity to have a P- conductivity type is epitaxially grown on a surface of the semiconductor substrate 10.

[0020] In a typical BiCMOS process, often a second lightly doped layer 16 (described in conjunction with Figure 1c below) is formed on the first layer 12. However, prior to the formation of the second lightly doped layer 16, in order to provide an isolation tank or region into which the vertical PNP transistor of the invention can be fabricated, a highly doped N type buried isolation region 18 (sometimes called a Diffusion Under Film or DUF layer) is formed in the first P type epitaxial layer 12. The DUF layer 18 will horizontally underlie the final PNP transistor structure to isolate a portion of the upper epitaxial layer 16, which will subsequently be formed, from the lower or bottom epitaxial region provided by the first epitaxial layer 12 and the substrate 10.

[0021] The DUF layer 18 may be formed by implanting a high concentration of a donor impurity, such as antimony, into a masked region (mask not shown) of the first epitaxial layer 12, as shown in Figure 1b. Then, an initial DUF diffusion is performed, partially driving the DUF impurity into the first eptiaxial layer 12.

[0022] The second epitaxial layer 16 is then formed over the first epitaxial layer 12 and the partially diffused DUF region, as shown in Figure 1c. The second epitaxial layer is lightly doped with an acceptor type impurity, such as boron, during its epitaxial growth to present an impurity level of about 2×10^{15} atoms/cm^3 to provide a layer having a P- type conductivity.

[0023] Following the formation of the second epitaxial layer 16, N+ wells 20 and 21 are formed to completely laterally isolate an island or tank region 22 of the upper epitaxial layer 16 in which the vertical PNP transistor will be formed. The N+ wells 20 and 21 may be formed by implanting the well regions with a high concentration level of a donor impurity, such as phosphorus, followed by sufficient impurity drive-in to drive the N type impurity ions to the underlying DUF region 18 (it should be noted that although two N+ wells 20 and 21 appear in the drawings, the physical configuration of the N+ well preferably would be a single region encircling or encompassing the interior semiconductor island, the two N+ well extents that intersect the cross-sectional view of the drawings only appearing as separate N+ well structures.) During the drive-in of the N+ well impurity, the underlying DUF region 18 will also be driven beyond the extents of its initial drive-in and into the upper epitaxial layer 16 and further into the lower epitaxial layer 12, so that, properly done, the DUF region 18 and the N+ well diffusions 20 and 21 join to completely isolate the island region 22 of the second epitaxial layer 16, as shown in Figure 1d.

[0024] One or more collector resistivity adjusting impurities are implanted and diffused into the second epitaxial layer 16 prior to the next step of diffusing the base impurity. One method by which such impurities may be implanted is shown in Figures 1e and 1f, which, as mentioned may be optionally performed as a part of the fabrication process by which the vertical PNP transistor of the invention is constructed. The process may be, for instance, a part of a standard LOCOS technique for field oxidation and implants. Thus, as shown in Figure 1e, the first step may be to form a layer of pad oxide 40 overall. Next, a layer of nitride 41 is formed, followed by a layer of photoresist 42. The photoresist layer 42 and the nitride layer 41 are patterned, essentially in an "inverse moat" pattern that defines the inverse layout of the features of the desired final PNP transistor. At this point, a donor impurity, such as phosphorous, is implanted into the areas of the epitaxial layer 16 exposed by the patterned nitride 41 and photoresist 42. A second layer of photoreisist 45, shown in Figure If, may then be formed over selected lower level photoresist/nitride features, or over the surface of the epitaxial layer 16 itself. Thus, for example, a second layer 45 of resist may be placed over the first layer of resist 42 and nitride 41 over the left N+ well 20, and entirely over the right N+ well 21. An acceptor impurity, such as boron, is then implanted into the exposed areas, counter doping the previously implanted donor impurity in common exposed regions, to become predominately P type. In regions that are masked by the second photoresist layer 45, on the other hand, the originally implanted donor impurity is seen, such as at the surface of the N+ well 21 and at the peripheral region of the surface of the N+ well 20. The resist layers 42 and 45, the nitride layer 41, and the pad oxide layer 40 are then removed.

[0025] The introduction of the resistivity adjusting implant is desirable because of the high collector resistance that may exist due to the epitaxial layer 16 being only lightly doped (in some cases, such boron implant may be performed as a part of a concurrently performed BiCMOS process step, such implant often being used, for instance, to increase the operating voltage of NPN transistors which also might be fabricated in some applications. An example of such process can be seen, for example, in U.S. Patent 4,855,244, assigned to the assignee hereof). One effect of the resistivity adjusting implant is to raise the doping level in the top several microns of the second epitaxial layer 16. As a result, the collector resistance of the PNP transistor will be reduced, and, in addition, the base width of the PNP transistor will be reduced, as can be seen from the graphs of Figures 2 and 3. The reduction in the width of the PNP transistor will result in a device with increased current gain (H_{fe}) and frequency threshold (F_t).

[0026] An isolation layer, which may conveniently be a field oxide layer 26 shown in Figure Ig, may then be

formed and patterned for the body and contact regions of the PNP transistor. Then, an N type base impurity is diffused into the tank or island 22 in the top epitaxial layer over the substrate to form the base region 28. The base impurity may be a donor impurity such as arsenic, antimony, or phosphorus. It should be noted that if the vertical PNP structure of the invention is constructed in conjunction with other BiCMOS structures, for example, structures involving tunnel diodes, or the like, the N type base impurity diffusion may also be used to form a tunnel diode region of such other structures, if desired.

[0027] After the formation of the base region 28, a P type emitter impurity 30 may be implanted and diffused into the base region to form the P+ emitter of the vertical PNP transistor, as shown in Figure 1h. The emitter impurity may be an acceptor impurity such as boron. Concurrently, a P+ collector contact region 34 also may be formed. Then, a donor type impurity may be implanted into regions 32 and 35 to provide an N+ base contact, and to afford an N+ DUF contact to enable the DUF and N+ wells, which underlie and surround the transistor structure, to be reverse biased, if desired, to assist in maintaining the isolation of the PNP device. It is noted that the N+ base contact region 32 may also be simultaneously performed with a source/drain implant/diffusion of an associated NMOS transistor, if the PNP transistor is being constructed as a part of a BiCMOS process.

[0028] As mentioned, it will be appreciated that since the processes for forming the various elements of the vertical PNP transistor may be similar to steps of a typical CMOS process, the steps for forming the vertical PNP transistor may be performed simultaneously during at least a portion of some BiCMOS processes if those processes have appropriate corresponding device structures. The cross sections of a few typically formed BiCMOS device structures are shown in Figures 4a and 4b, juxtaposed with a vertical PNP transistor constructed in accordance with the invention. In the structure illustrated in Figure 4a, for example, a standard isolated vertical PNP transistor 60 is shown fabricated in the same isolated island 61 as an isolated vertical PNP transistor 63 that has a collector resistivity implant 64 underlying its base. The collector resistivity implant is labeled "N well adj", since the implant may be performed, for example, concurrently with an N well adjust implant 68 in the formation of a high voltage NPN transistor 70. A standard vertical NPN transistor 71, which does not include an N well adjust implant, is shown adjacent the high voltage NPN transistor 70 for reference. Also, the base diffusion is labeled tunnel", since it can be performed concurrently with the formation of the tunnel implant and diffusion of the tunnel region of an accompanying EEPROM device 74.

[0029] Furthermore, the steps of forming the highly doped N type buried isolation regions 80 which underlie the islands in which the vertical PNP and NPN transistors are constructed can be simultaneously performed. Also, the implant and diffusion of the emitter impurity 82 of the vertical PNP transistor may be performed simultaneously with the formation of the source and drain regions 83 and 84 of an accompanying PMOS transistor 85 and an implant into regions 88 and 89 in base regions 91 and 93 for the respective high and low voltage NPN transistors 70 and 71. An NMOS transistor 86 is shown adjacent the PMOS transistor 85 for reference.

[0030] As shown in Figure 5, an isolated vertical PNP transistor 90, which does not include a collector resistivity adjusting implant, is shown. A donor impurity 92, such as phosphorus, is implanted or introduced adjacent the base region 94 to improve the voltage handling capability of the PNP transistor. It has been found, for example, that in an embodiment of a PNP transistor that has a voltage handling capability of about 25 volts, such implant can improve the voltage handling capability of the resulting PNP transistor to about 80 volts. The implant 92 can be accomplished, for example, by appropriate masking to define an area slightly larger than the area of the PNP transistor, during similar implantation of a donor impurity into the N well regions 98. Alternately, the doping may be accomplished by a blanket implant of the channel stop for N wells 98, followed by a counter doping implant with an acceptor impurity 99 in masked areas away from the region of the vertical PNP transistor 90.

[0031] One way by which the surface dopant may be implanted is by a process similar to that described above with reference to Figures 1e and 1f, as now shown in Figures 6a and 6b. With reference first to Figure 6a, the structure of Figure 5, before the formation of the surface oxidation and device elements is first coated with a layer of pad oxide 110 overall. A layer of nitride 111 and photoresist 112 are then also formed overall. The nitride 111 and photoresist 112 are then patterned in an "inverse moat" pattern, to expose the areas that will surround the features of the PNP transistor, and other areas desired to be implanted. As shown, a donor impurity, such as phosphorus, is implanted into the exposed areas.

[0032] Next, a second layer of photoresist 115 is selectively patterned over various desired features created by the first layer of photoresist 112 and nitride 111. For example, as shown in Figure 6b, the first layer 112 of photoresist and its accompanying underlying nitride layer 111 over the region 120 of the base of the transistor, over the region 122 of the left N+ well 123 and entirely over the region 125 of the right N+ well 126 may be covered with the patterned second layer of photoresist 115. Then, an acceptor impurity, such as boron, may be implanted into the exposed regions, counter doping the regions previously doped with the donor impurity, leaving the N channel stop regions adjacent the base of the transistor, the N surface regions of the right N+ well 126, and the N surface peripheral regions of the N+ well 123. The remaining exposed regions are P type. The pad oxide 110, nitride layer 112, and the first and second photoresist layers 112 and 115 are then removed.

Claims

1. A process for making a vertical PNP transistor, comprising the steps of:

   forming a highly doped N type buried isolation region (18) in a P type semiconductor substrate (10) to vertically isolate a top portion of said substrate from a bottom portion of said substrate by diffusing a N type impurity into a buried portion of said substrate;

   forming a highly doped N type isolation region (20, 21) to encompass and laterally isolate said top portion of said substrate;

   diffusing a N type base impurity into said encompassed top portion (22) of said substrate to form a base region (28);

   diffusing a P type emitter impurity into said base region (38) to form an emitter region (30) and, wherein said step of diffusing an N type impurity into a buried portion of said substrate comprises:

      forming a first lightly doped layer (12) of P type semiconductor material on a surface of a higly doped P type substrate (10);

      introducing a N type buried layer impurity into a surface region of said first lightly doped layer (12);

      forming a second lightly doped layer (16) of P type semiconductor material on said first lightly doped layer (12) and said buried layer impurity to provide said top portion of said substrate;

      diffusing said N type buried layer impurity into said first and second lightly doped layers (12, 16) of P type semiconductor material; and

      diffusing a P type collector resistivity adjusting impurity into a surface of the second lightly doped layer (16) prior to the step of diffusing the base impurity.

2. The process of claim 1, wherein said steps of forming the first and second lightly doped layers (12, 16) of P type semiconductor material comprise epitaxially growing said first and second layers (12, 16).

3. The process of claim 1, wherein said step of diffusing a base impurity comprises diffusing antimony into said second layer (16).

4. The process of claim 1, wherein said step of diffusing an emitter impurity comprises diffusing boron into said second layer (16).

5. The process of claim 1, further comprising the steps of forming base and emitter contact regions to the base and emitter impurities.

6. The process of claim 1, further comprising performing at least a portion of a BiCMOS process simultaneously with said steps of forming the N+ buried isolation region (18), diffusing the base impurity, and diffusing the emitter impurity.

7. The process of claim 6, wherein said BiCMOS process includes the step of forming an EEPROM (74) having a tunnel diode for charge transfer to a floating gate, and wherein said step of diffusing the base impurity is performed simultaneously with a tunnel diode diffusion.

Patentansprüche

1. Prozeß zum Herstellen eines vertikalen PNP-Transistors, der die folgenden Schritte umfaßt:

   Bilden eines stark dotierten vergrabenen N-Isolationsbereichs (18) in einem P-Halbleitersubstrat (10), um einen oberen Abschnitt des Substrats von einem unteren Abschnitt des Substrats vertikal zu isolieren, indem N-Störstellen in einen vergrabenen Abschnitt des Substrats diffundiert werden;

   Bilden eines stark dotierten N-Isolationsbereichs (20, 21), um den oberen Abschnitt des Substrats zu umschließen und seitlich zu isolieren;

   Diffundieren eines N-Basis-Störstoffs in den umschlossenen oberen Abschnitt (22) des Substrats, um einen Basisbereich (28) auszubilden;

   Diffundieren eines P-Emitter-Störstoffs in den Basisbereich (38), um einen Emitterbereich (30) auszubilden, wobei der Schritt des Diffundierens eines N-Störstoffs in einen vergrabenen Abschnitt des Substrats umfaßt:

      Bilden einer ersten schwach dotierten Schicht (12) eines P-Halbleitermaterials auf einer Oberfläche eines stark dotierten P-Substrats (10);

      Einleiten eines N-Störstoffs für eine vergrabene Schicht in einen Oberflächenbe-

reich der ersten schwach dotierten Schicht (12);

Bilden einer zweiten schwach dotierten Schicht (16) des P-Halbleitermaterials auf der ersten schwach dotierten Schicht (12) und auf dem Störstoff für die vergrabene Schicht, um den oberen Abschnitt des Substrats zu schaffen;

Diffundieren des N-Störstoffs für die vergrabene Schicht in die ersten und zweiten schwach dotierten Schichten (12, 16) des P-Halbleitermaterials; und

Diffundieren eines P-Kollektor-Störstoffs zur Einstellung des spezifischen elektrischen Widerstandes in eine Oberfläche der zweiten schwach dotierten Schicht (16) vor dem Schritt des Diffundierens des Basis-Störstoffs.

2. Prozeß nach Anspruch 1, bei dem die Schritte des Ausbildens der ersten und zweiten schwach dotierten Schichten (12, 16) des P-Halbleitermaterials das epitaktische Aufwachsen der ersten und zweiten Schichten (12, 16) umfassen.

3. Prozeß nach Anspruch 1, bei dem der Schritt des Diffundierens von Basisstörstellen das Diffundieren von Antimon in die zweite Schicht (16) umfaßt.

4. Prozeß nach Anspruch 1, bei dem der Schritt des Diffundierens des Emitter-Störstoffs das Diffundieren von Bor in die zweite Schicht (16) umfaßt.

5. Prozeß nach Anspruch 1, der ferner die Schritte des Ausbildens von Basisund Emitter-Kontaktbereichen in den Basis- und Emitter-Störstoffen umfaßt.

6. Prozeß nach Anspruch 1, der ferner das Ausführen wenigstens eines Teils eines BiCMOS-Prozesses gleichzeitig zu den Schritten des Ausbildens des vergrabenen N^+-Isolationsbereichs (18), des Diffundierens des Basis-Störstoffs und des Diffundierens des Emitter-Störstoffs umfaßt.

7. Prozeß nach Anspruch 6, bei dem der BiCMOS-Prozeß den Schritt des Ausbildens eines EEPROM (74), der eine Tunneldiode für die Ladungsverschiebung zu einem schwebenden Gate besitzt, umfaßt und bei dem der Schritt des Diffundierens des Basis-Störstoffs gleichzeitig mit einer Tunneldioden-Diffusion ausgeführt wird.

Revendications

1. Procédé pour la création d'un transistor PNP vertical comprenant les étapes suivantes :

   - une étape de formation d'une région d'isolation enterrée hautement dopée de type N (18) formée dans un substrat semi-conducteur de type P (10) pour isoler verticalement une portion supérieure dudit substrat d'une portion inférieure dudit substrat en diffusant des impuretés de type N dans une portion enterrée dudit substrat ;

   - une étape de formation d'une région d'isolation hautement dopée de type N (20, 21) pour englober et isoler latéralement ladite portion supérieure dudit substrat ;

   - une étape de diffusion d'une impureté de base de type N dans ladite portion supérieure englobée (22) dudit substrat pour former une région de base (28);

   - une étape de diffusion d'une impureté d'émetteur de type P dans ladite région de base (38) pour former une région d'émetteur (30) et, dans laquelle ladite étape de diffusion d'une impureté de type N dans une portion enterrée dudit substrat comprend :

   - une étape de formation d'une première couche (12) légèrement dopée formée de matériau semi-conducteur de type P sur une surface d'un substrat hautement dopée de type P (10);

   - une étape d'introduction d'une impureté de type N enterrée dans une couche, dans une région de surface de ladite première couche légèrement dopée (12);

   - une étape de formation d'une seconde couche (16) légèrement dopée formée d'un matériau semi-conducteur de type P sur ladite première couche légèrement dopée (12) et ladite impureté enterrée dans la couche pour fournir ladite portion supérieure dudit substrat ;

   - une étape de diffusion de ladite impureté de type N enterrée dans la couche dans lesdites première et seconde couches légèrement dopées formées d'un matériau semi-conducteur de type P ; et

   - une étape de diffusion d'une impureté d'ajustement de résistance de collecteur de type P dans une surface de la seconde couche légèrement dopée (16) avant l'étape de diffusion d'une impureté de base.

2. Procédé selon la revendication 1, dans lequel lesdites étapes de formation des première et seconde couches (12,16) légèrement dopée de matériau semi-conducteur de type P comprennent une étape de développement épitaxial desdites première et seconde couches (12,16).

3. Procédé selon la revendication 1, dans lequel ladite étape de diffusion d'une impureté de base comprend la diffusion d'antimoine dans la seconde couche (16).

4. Procédé selon la revendication 1, dans lequel ladite étape de diffusion d'une impureté d'émetteur comprend la diffusion de bore dans ladite seconde couche (16)

5. Procédé selon la revendication 1, comprenant en outre les étapes de formation de régions de contact de base et d'émetteur sur les impuretés de base et d'émetteur.

6. Procédé selon la revendication 1, comprenant en outre une étape de réalisation d'au moins une portion d'un procédé BiCMOS simultanément avec ladite étape de formation de la région d'isolation enterrée de type N (18), en diffusant l'impureté de base et en diffusant l'impureté d'émetteur.

7. Procédé selon la revendication 6, dans lequel ledit procédé BiCMOS comprend une étape de formation d'une EEPROM (74) ayant une diode tunnel pour le transfert de charges vers une grille flottante, dans lequel ladite étape de diffusion de l'impureté de base est réalisée simultanément avec la diffusion d'une diode tunnel.

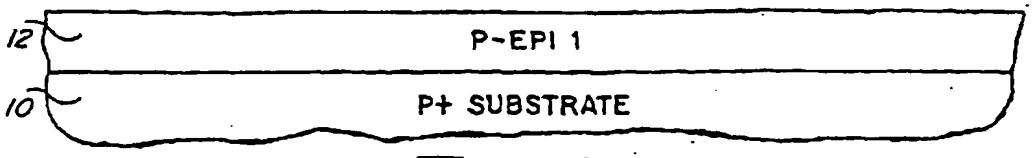

FIG.1a

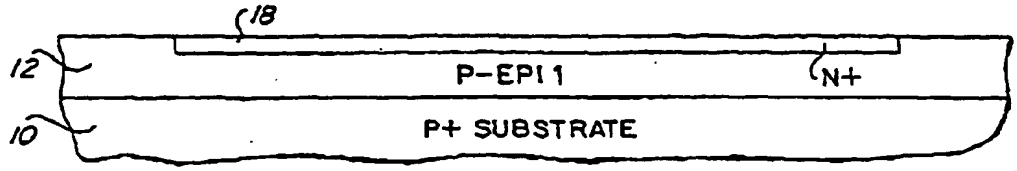

FIG.1b

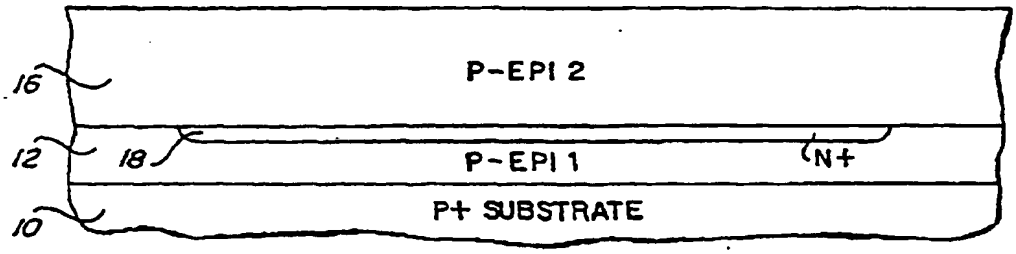

FIG.1c

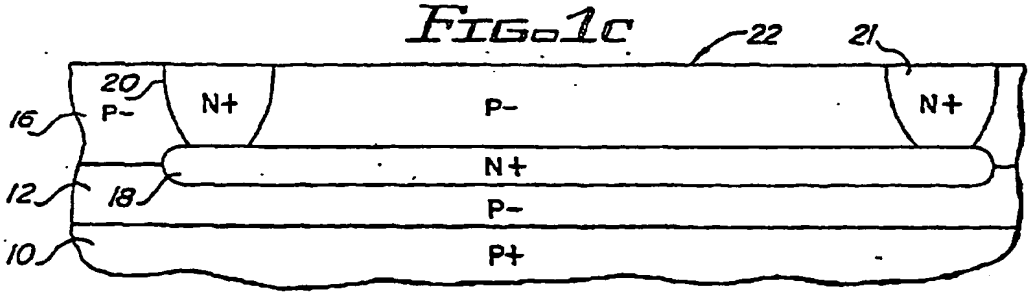

FIG.1d

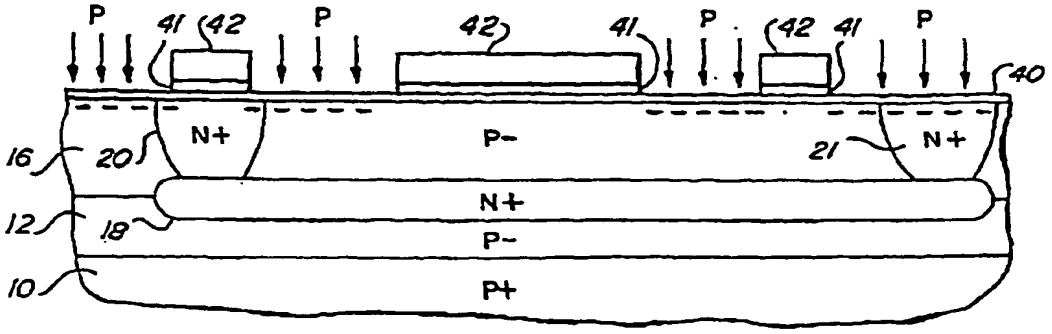

FIG.1e

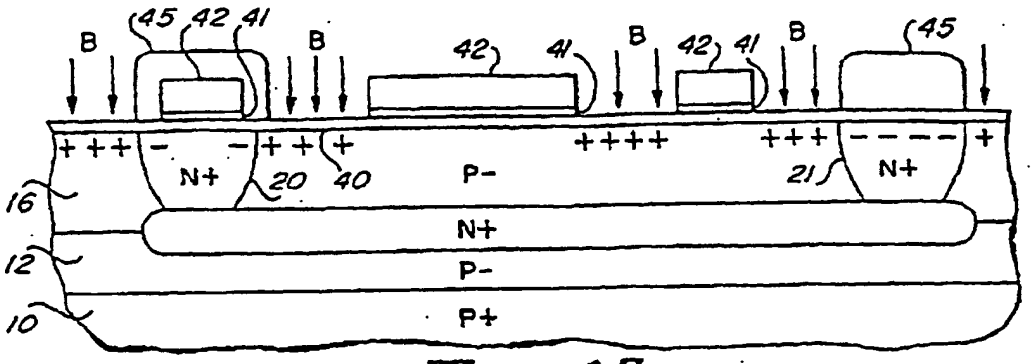

FIG. 1f

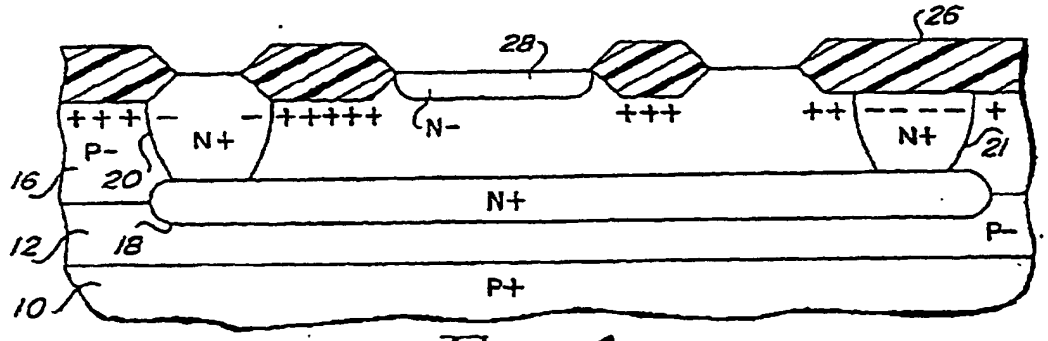

FIG. 1g

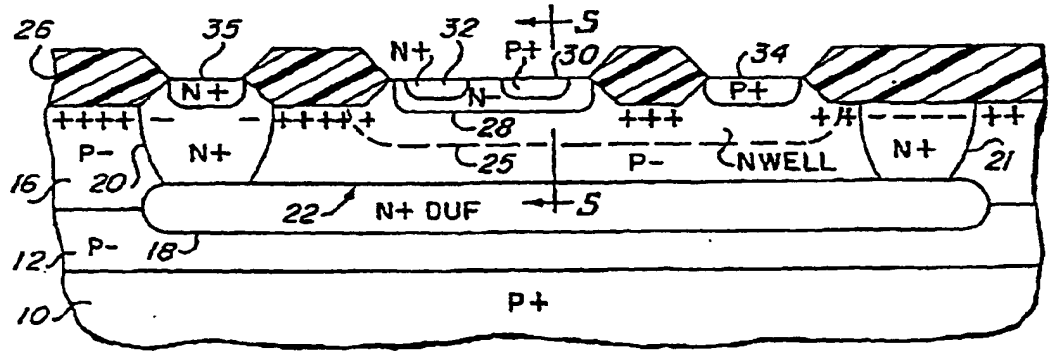

FIG. 1h

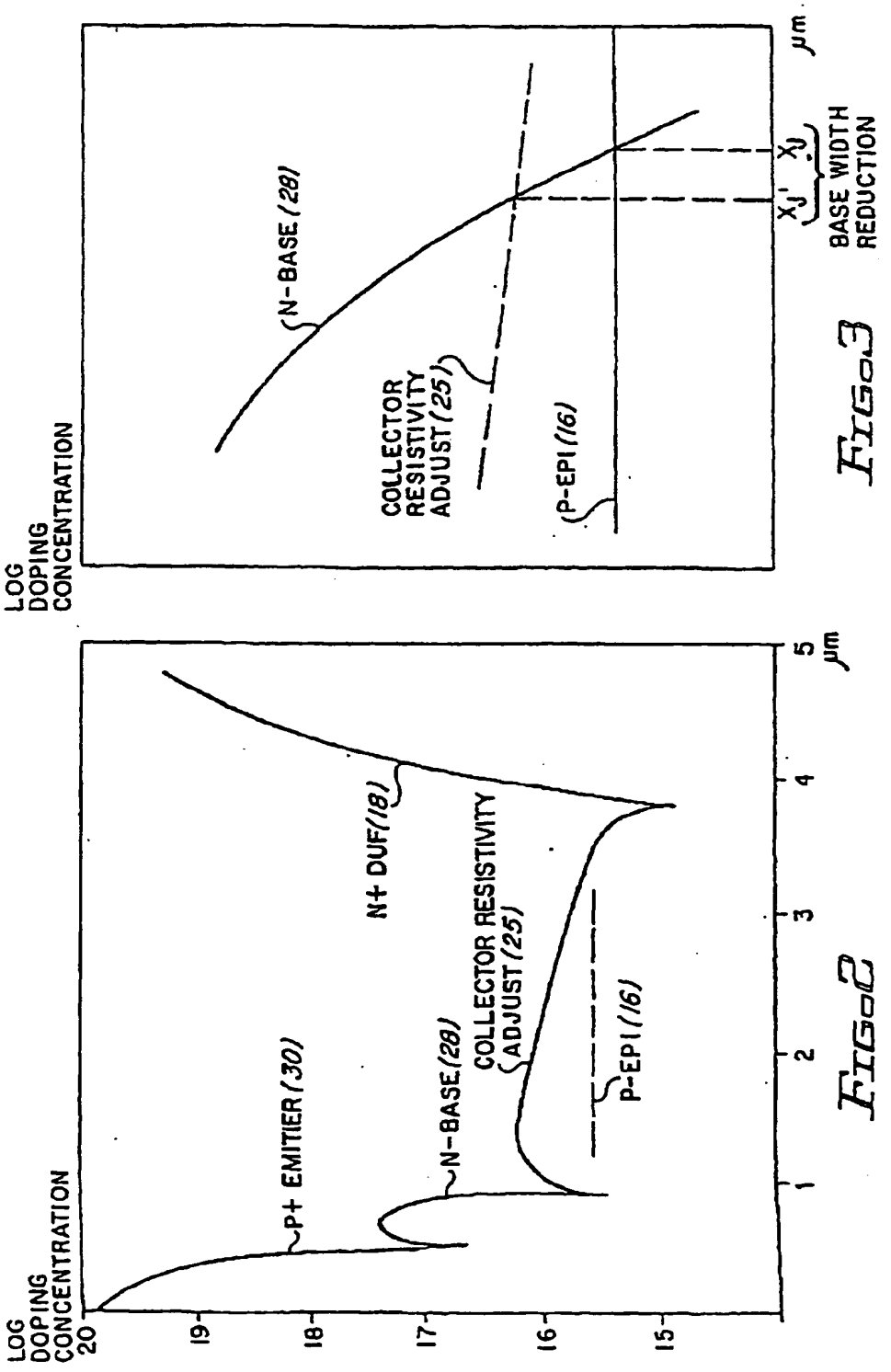
LOG
DOPING
CONCENTRATION
20
19
18
17
16
15
P+ EMITIER (30)
N+ DUF (18)
N-BASE (28)
COLLECTOR RESISTIVITY
ADJUST (25)
P-EPI (16)
1
2
3
4
5
μm

Fig. 2

LOG
DOPING
CONCENTRATION
N-BASE (28)
COLLECTOR
RESISTIVITY
ADJUST (25)
P-EPI (16)
X_J' X_J
BASE WIDTH
REDUCTION
μm

Fig. 3

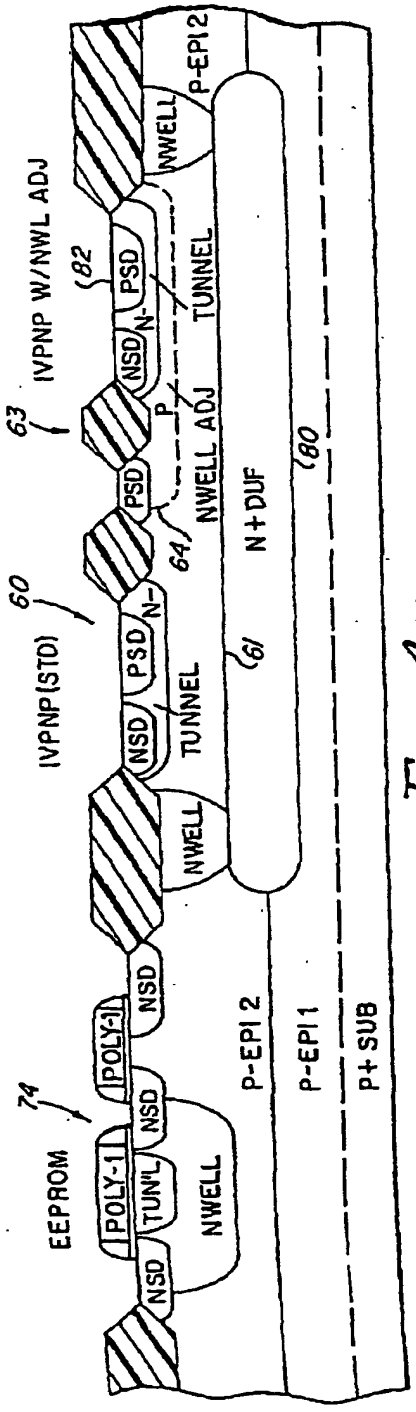
EEPROM
74
POLY-1
TUN'L
NSD
NWELL
NSD
POLY-1
NSD
P-EPI 2
P-EPI 1
P+ SUB
IVPNP(STD)
60
NSD
PSD
N-
TUNNEL
NWELL
61
IVPNP W/NWL ADJ
63
PSD
N-
64
NWELL ADJ
P
NSD
PSD
N
82
TUNNEL
NWELL
P-EPI2
N+ DUF
80

Fig. 4a

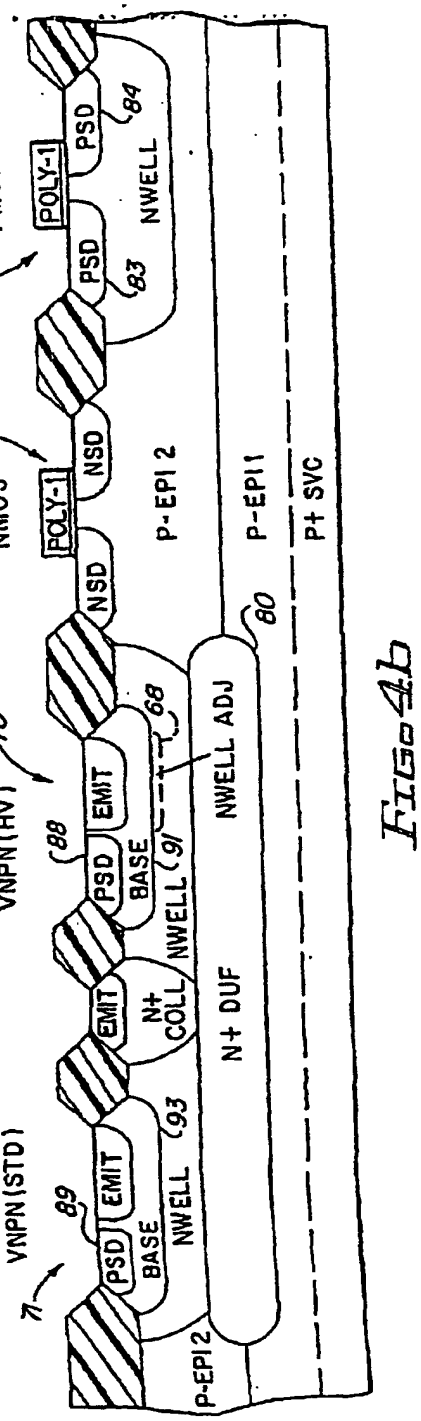
VNPN(STD)
71
89
PSD
EMIT
BASE
NWELL
93
EMIT
N+
COLL
NWELL
91
PSD
EMIT
BASE
88
VNPN(HV)
70
NSD
POLY-1
NSD
68
NWELL ADJ
NMOS
86
POLY-1
PSD
NSD
P-EPI 2
80
PMOS
85
POLY-1
PSD
PSD
83
NWELL
84
P-EPI1
P+ SVC
N+ DUF
P-EPI2

Fig. 4b

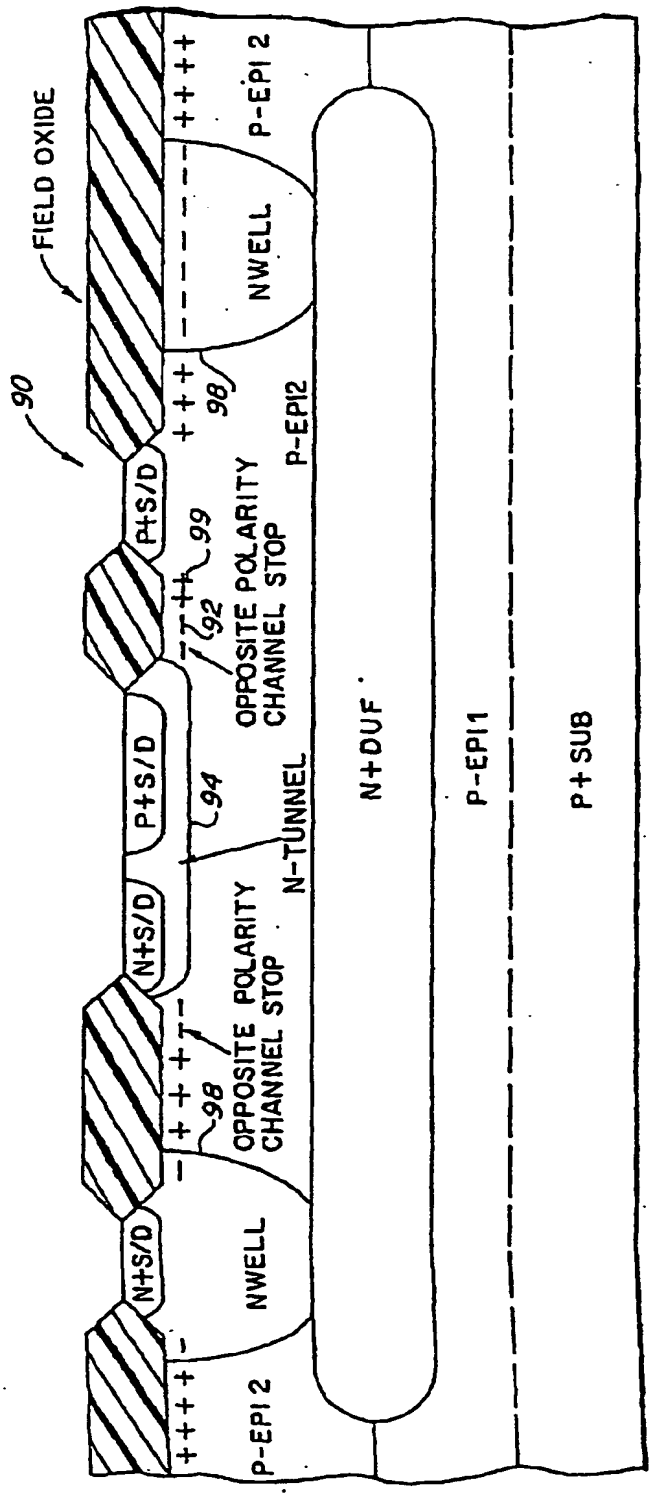
FIELD OXIDE
90
P-EPI 2
NWELL
98
P-EPI2
P+S/D
99
92
OPPOSITE POLARITY
CHANNEL STOP
P+S/D
94
N-TUNNEL
N+S/D
OPPOSITE POLARITY
CHANNEL STOP
98
N+S/D
NWELL
P-EPI 2
N+DUF
P-EPI1
P+ SUB

FIG. 5

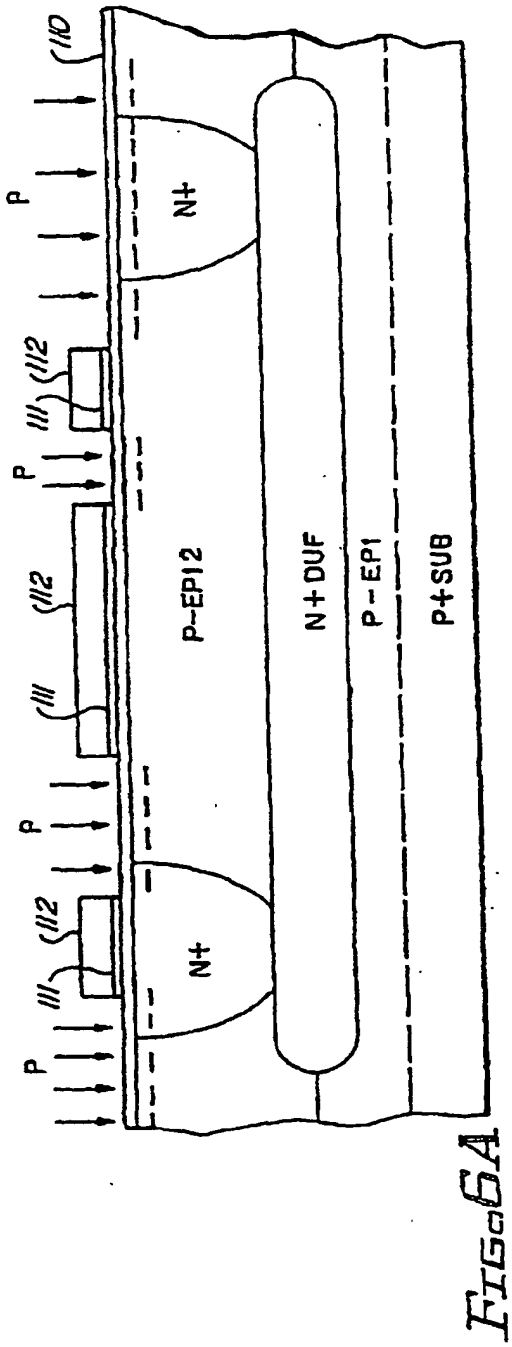
110
P
112
111
N+
P-EPI2
N+DUF
P-EPI
P+SUB

Fig.6A

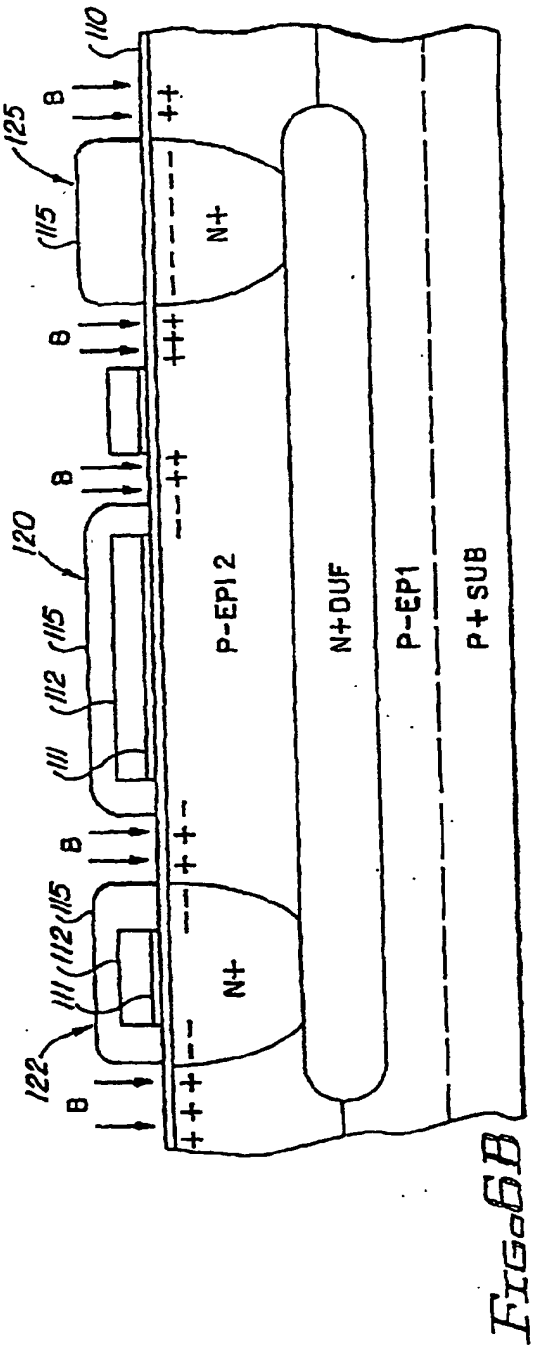
110
125
B
115
112
111
120
122
N+
P-EPI2
N+DUF
P-EPI
P+SUB

Fig.6B